In re Patent Application of:
CROCE ET AL.
Serial No. **09/839,596**
Filing Date: **4/20/01**

In the Claims:

Claims 1-4 (Cancelled).

5. (Currently amended) A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

a body region completely surrounded on a bottom and sides thereof by said buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

6. (Original) The LDMOS integrated device of Claim 5 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

7. (Original) The LDMOS integrated device of Claim 5 wherein the portions of said drain region adjacent said superficial buffer region have a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3}.

8. (Original) The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a depth of about 0.15 to 0.45 micrometers.

9. (Original) The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3}.

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10. (Original) The LDMOS integrated device of Claim 5 wherein said body region has a depth of about 0.25 to 0.75 micrometers.

11. (Original) The LDMOS integrated device of Claim 5 wherein said body region has a dopant concentration of about $5x10^{17}$ to $5x10^{18}$ atoms cm^{-3}.

12. (Original) The LDMOS integrated device of Claim 5 wherein said drain region is doped with phosphorous; and wherein said body region is doped with boron.

13. (Original) The LDMOS integrated device of Claim 5 wherein said drain region is doped with boron; and wherein said body region is doped with phosphorus.

14. (Currently amended) A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial buffer region being more heavily doped than adjacent portions of said drain region;

said superficial buffer region having a dopant concentration of about $5x10^{16}$ to $5x10^{17}$ atoms cm^{-3} and the adjacent portions of said drain region having a dopant concentration of about $2.5x10^{15}$ to $2.5x10^{16}$ atoms cm^{-3};

a body region completely surrounded on a bottom and sides thereof by said superficial buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

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15. (Original) The LDMOS integrated device of Claim 14 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

16. (Original) The LDMOS integrated device of Claim 14 wherein said buffer region has a depth of about 0.15 to 0.45 micrometers.

17. (Original) The LDMOS integrated device of Claim 14 wherein said body region has a depth of about 0.25 to 0.75 micrometers.

18. (Original) The LDMOS integrated device of Claim 14 wherein said body region has a dopant concentration of about $5x10^{17}$ to $5x10^{18}$ atoms cm^{-3}.

19. (Withdrawn).

20. (Withdrawn)

21. (Withdrawn).

22. (Withdrawn).

23. (Withdrawn).

24. (Withdrawn).

25. (Withdrawn).